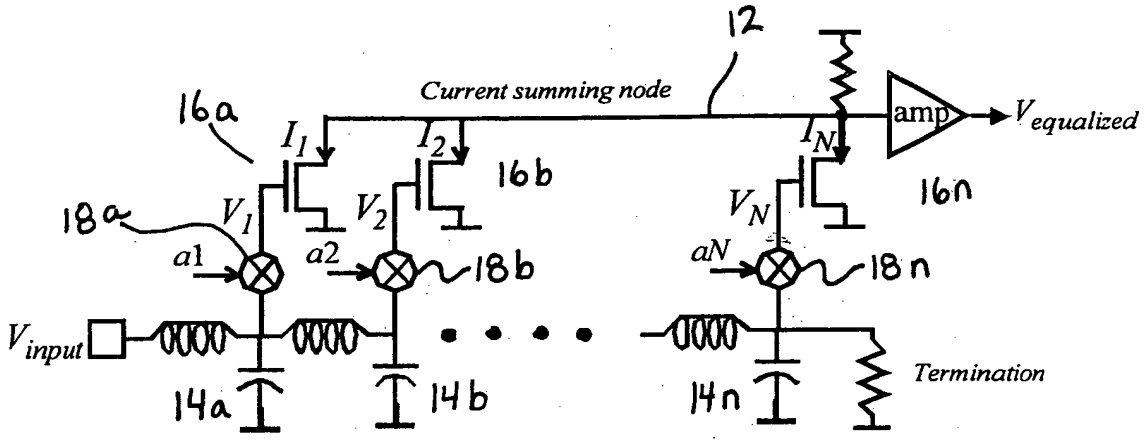
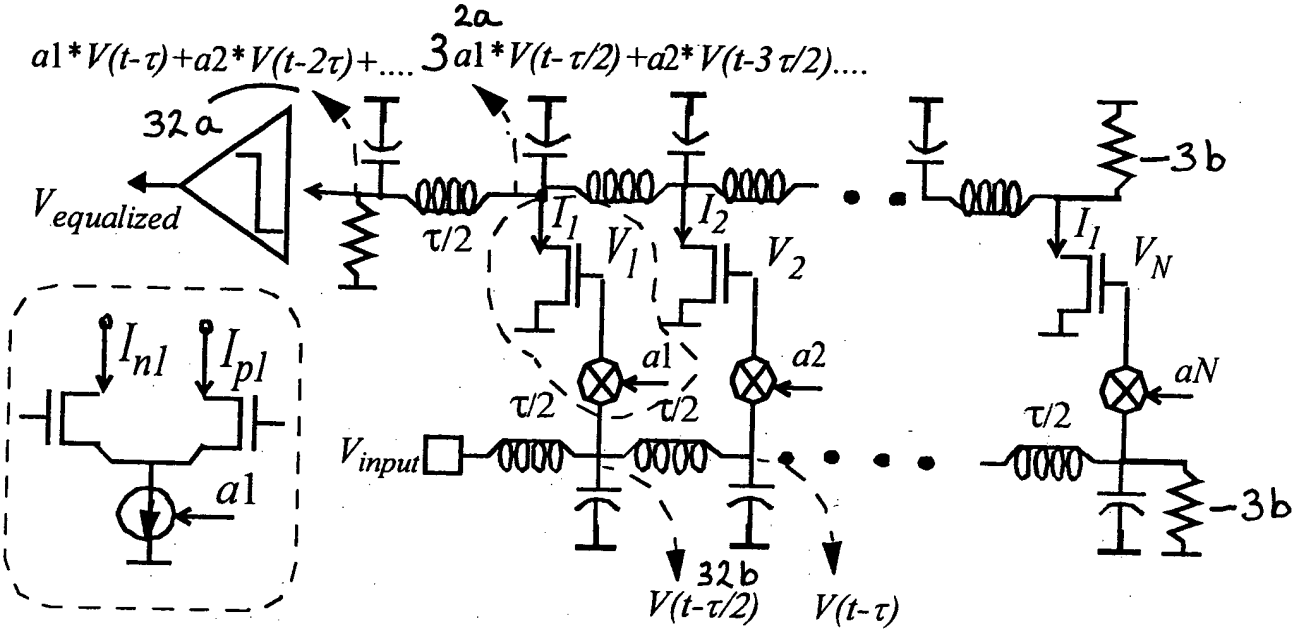

12
Current summing node
16a
I_1
I_2
I_N
amp
$V_{equalized}$
16b
16n
18a
V_1
V_2
V_N
a1
a2
aN
18b
18n
V_{input}
Termination
14a
14b
14n

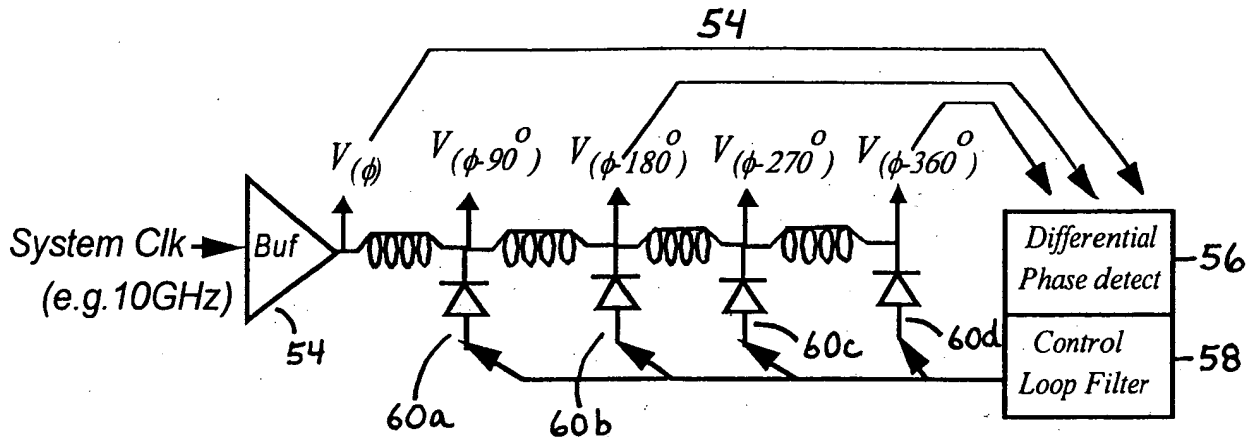
10

Fig. 1


a1*V(t-τ)+a2*V(t-2τ)+....
2a
3a1*V(t-τ/2)+a2*V(t-3τ/2)....
32a
V equalized
τ/2
I1
V1
I2
V2
3b
I1
VN
Inl
Ipl
a1
a2
aN
τ/2
τ/2
τ/2
Vinput
a1
3b
32b
V(t-τ/2)
V(t-τ)

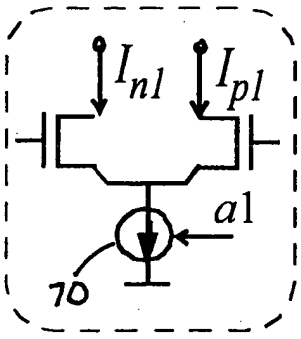
30

Fig. 2


54
$V_{(\phi)}$
$V_{(\phi-90^o)}$
$V_{(\phi-180^o)}$
$V_{(\phi-270^o)}$
$V_{(\phi-360^o)}$
System Clk
(e.g.10GHz)
Buf
54
60a
60b
60c
60d
Differential
Phase detect
56
Control
Loop Filter
58

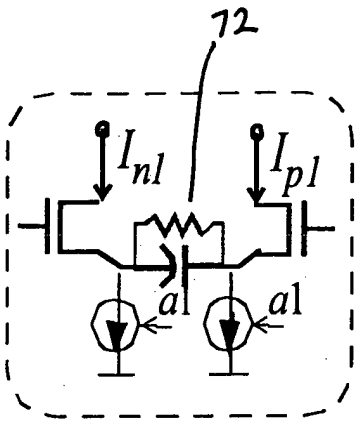
50

Fig. 3



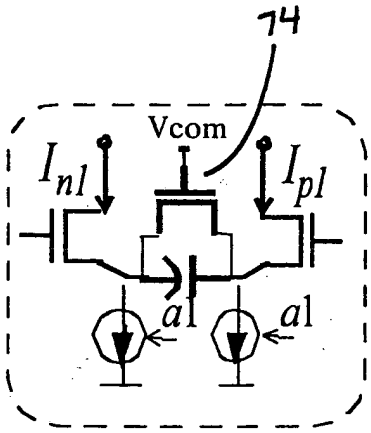
(a)

Fig. 4A



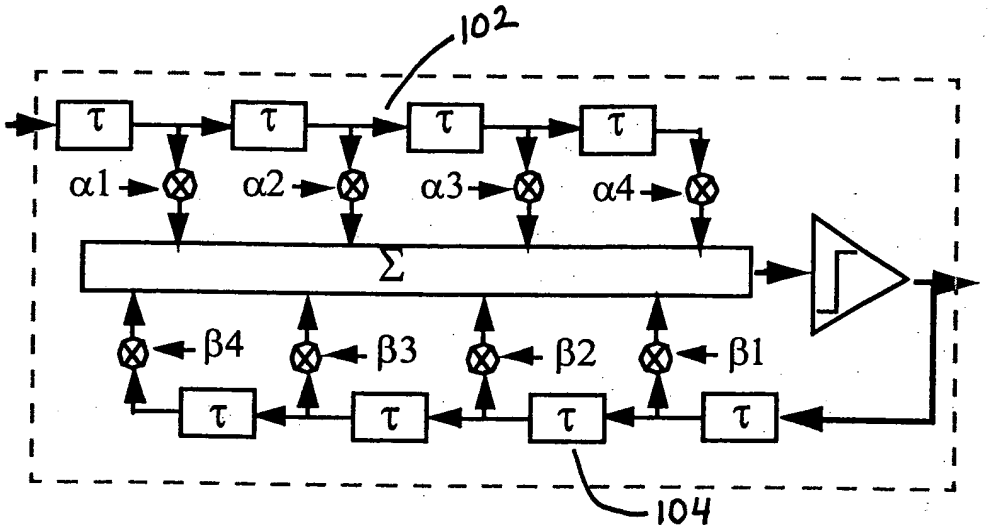
(b)

Fig. 4B



(c)

Fig. 4C



100

Fig. 5

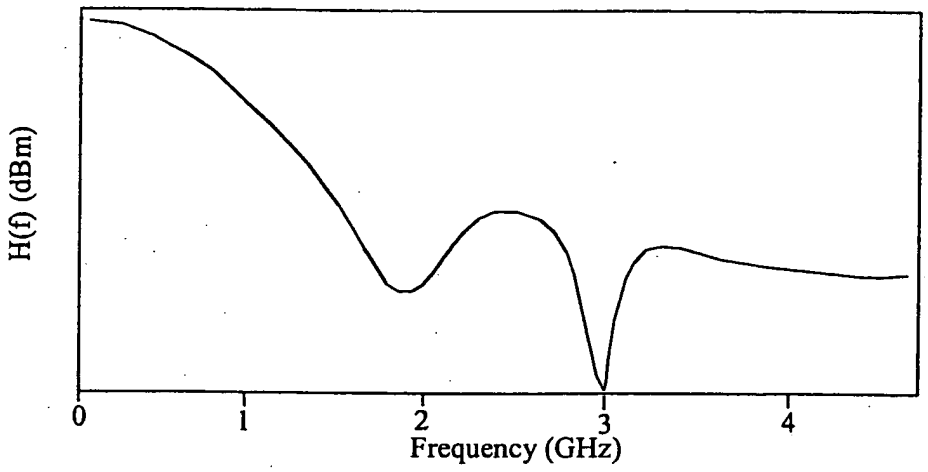


Fig. 6

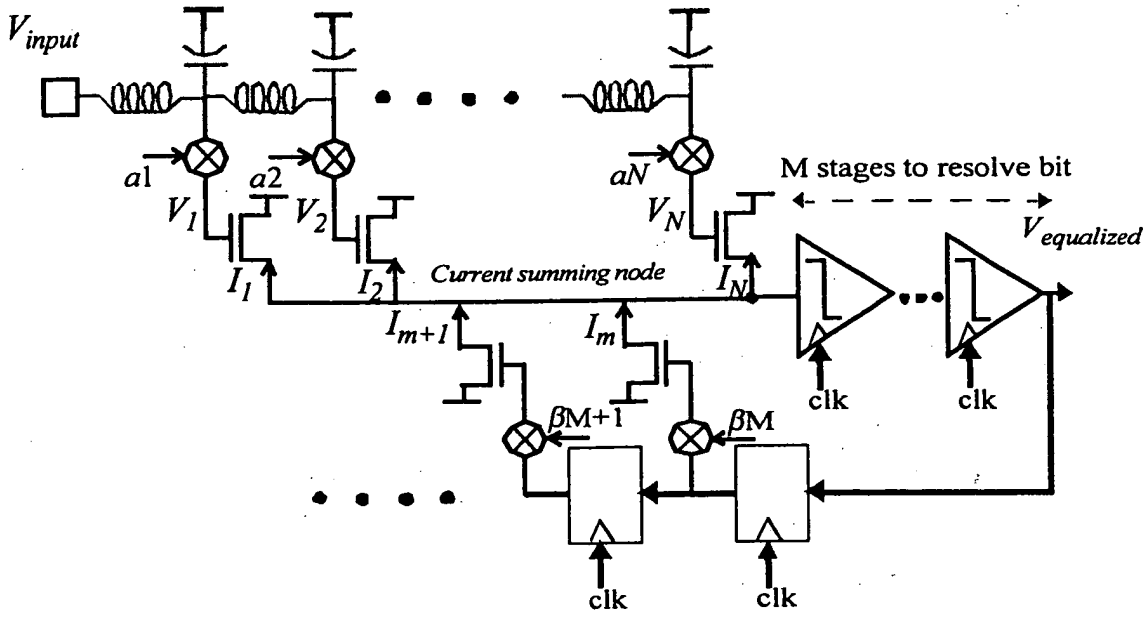

V_{input}
a1
a2
aN
V_1
V_2
V_N
M stages to resolve bit
$V_{equalized}$
I_1
I_2
Current summing node
I_N
I_{m+1}
I_m
clk
clk
βM+1
βM
clk
clk

Fig. 7